

# *Personal Systems Reference*

## *PC Processors*

*August 2005 - Version 295*

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# [Mobile] Intel Celeron M Processor

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Personal Systems Reference (PSREF)

## Intel® Celeron® M processor for mobile systems

Code name	Banias Celeron or ICP-M
Messaging	Based on an architecture designed specifically for mobile computing, the Intel Celeron M processor delivers a balanced level of mobile processor technology and exceptional value in sleeker, lighter notebook designs
Micro-architecture	IA-32 / micro-op fusion, dedicated stack manager, advanced branch prediction, power-optimized processor system bus
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
Power mgmt technology	Auto Halt, Stop Grant, Deep Sleep, Deeper Sleep

L1 cache - bus	256-bit data path / full speed
L1 data cache	32KB data cache / integrated
L1 instruction cache	32KB instruction cache / integrated

L2 cache - size	<b>512KB</b> / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (internal die; on die)
L3 cache	None

System bus	<b>400MHz</b> (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
System bus - width	64-bit data path

Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit
Out-of-order instructions	Yes (out-of-order instruction execution)
Branch prediction	Dynamic (based on history)
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit

Compatibility	Compatible with IA-32 software
Multiple processors	No SMP support

Technology (micron)	0.13u
Package and connector	<b>Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)</b>

		<i>Voltage</i>	<i>Thermal Design Power</i>	<i>Announce date</i>
Frequency (MHz/GHz) and available date	<b>800MHz Ultra Low Voltage</b>	<b>1.004 volts</b>	<b>7 watts</b>	January 2004
	<b>900MHz Ultra Low Voltage</b>	<b>1.004 volts</b>	<b>7 watts</b>	April 2004
	<b>1.2GHz</b>	<b>1.356 volts</b>	<b>24.5 watts</b>	January 2004
	<b>1.3GHz</b>	<b>1.356 volts</b>	<b>24.5 watts</b>	January 2004
	<b>1.4GHz</b>	<b>1.356 volts</b>	<b>24.5 watts</b>	April 2004

Chipset support	<b>Intel 855 chipset family</b> <b>Intel 852GM</b> <b>Other compatible chipsets</b>
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# [Mobile] Intel Celeron M Processor 3xx

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<b>Intel® Celeron® M processor for mobile systems</b>							
	Clock speed	L2 cache	Execute Disable Bit	System bus	Hyper-Threading Technology	Available date	
Intel Celeron M Processor Ultra Low Voltage 353	900MHz	512KB	No	400MHz	No	July 2004	
Intel Celeron M Processor Ultra Low Voltage 373	1.0GHz	512KB	<b>Yes</b>	400MHz	No	January 2005	
Intel Celeron M Processor Ultra Low Voltage 383	1.0GHz	<b>1MB</b>	<b>Yes</b>	400MHz	No	April 2005	
Intel Celeron M Processor 310	1.2GHz	512KB	No	400MHz	No	January 2004	
Intel Celeron M Processor 320	1.3GHz	512KB	No	400MHz	No	January 2004	
Intel Celeron M Processor 330	1.4GHz	512KB	No	400MHz	No	April 2004	
Intel Celeron M Processor 340	1.5GHz	512KB	No	400MHz	No	June 2004	
Intel Celeron M Processor 350	1.3GHz	<b>1MB</b>	No	400MHz	No	August 2004	
Intel Celeron M Processor 350J	1.3GHz	<b>1MB</b>	<b>Yes</b>	400MHz	No	August 2004	
Intel Celeron M Processor 360	1.4GHz	<b>1MB</b>	No	400MHz	No	August 2004	
Intel Celeron M Processor 360J	1.4GHz	<b>1MB</b>	<b>Yes</b>	400MHz	No	August 2004	
Intel Celeron M Processor 370	1.5GHz	<b>1MB</b>	<b>Yes</b>	400MHz	No	January 2005	
Intel Celeron M Processor 380	1.6GHz	<b>1MB</b>	<b>Yes</b>	400MHz	No	July 2005	
Code name	Banias Celeron or ICP-M						
Messaging	Based on an architecture designed specifically for mobile computing, the Intel Celeron M processor delivers a balanced level of mobile processor technology and exceptional value in sleeker, lighter notebook designs						
Micro-architecture	IA-32 / micro-op fusion, dedicated stack manager, advanced branch prediction, power-optimized processor system bus						
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)						
SSE2	Streaming SIMD Extensions 2 (144 new instructions)						
SSE3	No						
Hyper-Threading	No						
Power mgmt technology	Auto Halt, Stop Grant, Deep Sleep, Deeper Sleep						
Execute Disable Bit	<i>Some:</i> protects memory data from malicious software execution						
L1 cache - bus	256-bit data path / full speed						
L1 data cache	32KB data cache / integrated						
L1 instruction cache	32KB instruction cache / integrated						
L2 cache - size	<b>512KB</b> or <b>1MB</b> / full speed (Advanced Transfer Cache)						
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (internal die; on die)						
L3 cache	None						
System bus	<b>400MHz</b> (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size						
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz						
System bus - width	64-bit data path						
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit						
Out-of-order instructions	Yes (out-of-order instruction execution)						
Branch prediction	Dynamic (based on history)						
Speculative execution	Yes (Advanced Dynamic Execution)						
Math coprocessor	Pipelined floating point unit						
Compatibility	Compatible with IA-32 software						
Process technology	310 to 340: 130nm (nanometer) or 0.13u (micron); 350 to 360: 90nm or 0.09u						
Package and connector	<b>Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)</b>						
Frequency	353:	<b>900MHz Ultra Low Voltage</b>		<b>0.0940 volts</b>	<b>5 watts</b>		
	373/383:	<b>1.0GHz Ultra Low Voltage</b>		<b>0.0940 volts</b>	<b>5 watts</b>		
	310:	<b>1.2GHz</b>		<b>1.356 volts</b>	<b>24.5 watts</b>		
	320:	<b>1.3GHz</b>		<b>1.356 volts</b>	<b>24.5 watts</b>		
	330:	<b>1.4GHz</b>		<b>1.356 volts</b>	<b>24.5 watts</b>		
	340:	<b>1.5GHz</b>		<b>1.356 volts</b>	<b>24.5 watts</b>		
	350/350J:	<b>1.3GHz</b>		<b>1.260 volts</b>	<b>21 watts</b>		
	360/360J:	<b>1.4GHz</b>		<b>1.260 volts</b>	<b>21 watts</b>		
	370:	<b>1.5GHz</b>		<b>1.260 volts</b>	<b>21 watts</b>		
	380:	<b>1.6GHz</b>		<b>1.260 volts</b>	<b>21 watts</b>		
Chipset support	<b>Intel 852GM chipset</b> <b>Intel 855 chipset family</b> <b>Mobile Intel 910GML Express Chipset</b> <b>Mobile Intel 915 Express Chipset family</b> <b>Other compatible chipsets</b>						

# Mobile Intel Pentium 4 Processor 5xx

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## Mobile Intel® Pentium® 4 processor for mobile systems

	Clock speed	L2 cache	Execute Disable Bit	System bus	Hyper-Threading Technology	Available date
Mobile Intel Pentium 4 Processor 518	2.8GHz	1MB	No	533MHz	Hyper-Threading Technology	June 2004
Mobile Intel Pentium 4 Processor 532	3.06GHz	1MB	No	533MHz	Hyper-Threading Technology	June 2004
Mobile Intel Pentium 4 Processor 538	3.2GHz	1MB	No	533MHz	Hyper-Threading Technology	June 2004
Mobile Intel Pentium 4 Processor 548	3.33GHz	1MB	No	533MHz	Hyper-Threading Technology	September 2004
Mobile Intel Pentium 4 Processor 552	3.46GHz	1MB	No	533MHz	Hyper-Threading Technology	January 2005
Messaging	Second generation Mobile Intel Pentium 4 processor designed for larger-sized notebooks also known as "desktop replacements" typically featuring large screens, full-size keyboards, and multiple drives					
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)					
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)					
SSE2	Streaming SIMD Extensions 2 (144 new instructions)					
SSE3	Streaming SIMD Extensions 3 (13 new instructions)					
Hyper-Threading	Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)					
Power mgmt technology	Enhanced Intel SpeedStep™ technology, Auto Halt, Stop Grant, Deep Sleep, Deeper Sleep					
Execute Disable Bit	No					
L1 cache - bus	256-bit data path / full speed					
L1 data cache	16KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated					
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)					
L2 cache - size	<b>1MB</b> / full speed (Advanced Transfer Cache)					
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC					
L3 cache	None					
System bus	<b>533MHz</b> (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size					
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 266MHz					
System bus - width	64-bit data path					
Execution units	2 integer units; 1 floating point unit; 1 load unit; 1 store unit					
Out-of-order instructions	Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)					
Branch prediction	Yes (out-of-order instruction execution)					
Speculative execution	Dynamic (based on history) / 4KB Branch Target Buffer					
Math coprocessor	Yes (Advanced Dynamic Execution)					
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers					
Compatibility	Compatible with IA-32 software					
Multiple processors	No SMP support					
Other features	Thermal monitoring, built-in self test, IEEE 1149.1 standard test access port and boundary scan					
Process technology	90nm (nanometer) or 0.09u (micron)					
Package and connector	<b>Flip-Chip Pin Grid Array (FC-mPGA4) package</b> <b>requires 478-pin surface mount Zero Insertion Force (ZIF) socket (mPGA478B socket)</b>					
Frequency	<b>2.8GHz</b>	<i>Performance Mode</i>		<i>Battery Mode</i>		
	<b>3.06GHz</b>	<b>2.8GHz, 88 watts at 1.25-1.40 volts</b>		<b>1.86GHz, 1.15 volts</b>		
	<b>3.2GHz</b>	<b>3.06GHz, 88 watts at 1.25-1.40 volts</b>		<b>1.86GHz, 1.15 volts</b>		
	<b>3.33GHz</b>	<b>3.2GHz, 88 watts at 1.25-1.40 volts</b>		<b>1.86GHz, 1.15 volts</b>		
	<b>3.46GHz</b>	<b>3.33GHz, 88 watts at 1.25-1.40 volts</b>		<b>1.86GHz, 1.15 volts</b>		
		<b>3.46GHz, 88 watts at 1.25-1.40 volts</b>		<b>1.86GHz, 1.15 volts</b>		
Chipset support	<b>Intel 852GME, 852PM chipsets</b> <b>Other compatible chipsets</b>					

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# [Mobile] Intel Pentium M Processor

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## Intel® Pentium® M processor for mobile systems

Code name	<b>Banias</b>			
Branding	Part of the Intel Centrino™ mobile technology when included with an Intel 855 family chipset and Intel PRO/Wireless Network Connection wireless chip			
Micro-architecture	IA-32 / micro-op fusion, dedicated stack manager, advanced branch prediction, power-optimized processor system bus			
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)			
SSE2	Streaming SIMD Extensions 2 (144 new instructions)			
Power mgmt technology	Enhanced Intel SpeedStep™ technology, Auto Halt, Stop Grant, Deep Sleep, Deeper Sleep			
L1 cache - bus	256-bit data path / full speed			
L1 data cache	32KB data cache / integrated			
L1 instruction cache	32KB instruction cache / integrated			
L2 cache - size	<b>1MB</b> / full speed (Advanced Transfer Cache)			
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (internal die; on die)			
L3 cache	None			
System bus	<b>400MHz</b> (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size			
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz			
System bus - width	64-bit data path			
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit			
Out-of-order instructions	Yes (out-of-order instruction execution)			
Branch prediction	Dynamic (based on history)			
Speculative execution	Yes (Advanced Dynamic Execution)			
Math coprocessor	Pipelined floating point unit			
Compatibility	Compatible with IA-32 software			
Multiple processors	No SMP support			
Technology (micron)	0.13u			
Package and connector	<b>Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)</b>			
Frequency (MHz/GHz) and available date		<i>Highest Frequency Mode</i>	<i>Lowest Frequency Mode</i>	<i>Announce date</i>
	<b>900MHz Ultra Low Voltage</b>	<b>900MHz at 1.0 volts</b>	<b>600MHz at 0.85 volts</b>	March 2003
	<b>1.0GHz Ultra Low Voltage</b>	<b>1.0GHz at 1.0 volts</b>	<b>600MHz at 0.85 volts</b>	June 2003
	<b>1.1GHz Ultra Low Voltage</b>	<b>1.1GHz at 1.0 volts</b>	<b>600MHz at 0.85 volts</b>	April 2004 (also Pentium M 713)
	<b>1.1GHz Low Voltage</b>	<b>1.1GHz at 1.18 volts</b>	<b>600MHz at 0.96 volts</b>	March 2003
	<b>1.2GHz Low Voltage</b>	<b>1.2GHz at 1.18 volts</b>	<b>600MHz at 0.96 volts</b>	June 2003
	<b>1.3GHz Low Voltage</b>	<b>1.3GHz at 1.18 volts</b>	<b>600MHz at 0.96 volts</b>	April 2004 (also Pentium M 718)
	<b>1.3GHz</b>	<b>1.3GHz at 1.5 volts</b>	<b>600MHz at 0.96 volts</b>	March 2003
	<b>1.4GHz</b>	<b>1.4GHz at 1.5 volts</b>	<b>600MHz at 0.96 volts</b>	March 2003
	<b>1.5GHz</b>	<b>1.5GHz at 1.5 volts</b>	<b>600MHz at 0.96 volts</b>	March 2003
	<b>1.6GHz</b>	<b>1.6GHz at 1.5 volts</b>	<b>600MHz at 0.96 volts</b>	March 2003
	<b>1.7GHz</b>	<b>1.7GHz at 1.5 volts</b>	<b>600MHz at 0.96 volts</b>	June 2003
Chipset support	<b>Intel 855 chipset family with DDR-SDRAM memory</b> <b>Other compatible chipsets</b>			

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# [Mobile] Intel Pentium M Processor 7xx

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## Intel® Pentium® M processor for mobile systems

	Clock speed Performance Mode	Clock speed Battery Mode	L2 cache	Execute Disable Bit	System bus	Technology	Available date
Intel Pentium M Processor Ultra Low Voltage 713	1.10GHz	600MHz	<b>1MB</b>	No	400MHz	130nm	April 2004
Intel Pentium M Processor Ultra Low Voltage 723	1.00GHz	600MHz	2MB	No	400MHz	90nm	July 2004
Intel Pentium M Processor Ultra Low Voltage 733	1.10GHz	600MHz	2MB	No	400MHz	90nm	July 2004
Intel Pentium M Processor Ultra Low Voltage 733J	1.10GHz	600MHz	2MB	<b>Yes</b>	400MHz	90nm	August 2004
Intel Pentium M Processor Ultra Low Voltage 753	1.20GHz	600MHz	2MB	<b>Yes</b>	400MHz	90nm	January 2005
Intel Pentium M Processor Low Voltage 718	1.30GHz	600MHz	<b>1MB</b>	No	400MHz	130nm	April 2004
Intel Pentium M Processor Low Voltage 738	1.40GHz	600MHz	2MB	No	400MHz	90nm	July 2004
Intel Pentium M Processor Low Voltage 758	1.50GHz	600MHz	2MB	<b>Yes</b>	400MHz	90nm	January 2005
Intel Pentium M Processor Low Voltage 778	1.60GHz	600MHz	2MB	<b>Yes</b>	400MHz	90nm	July 2005
Intel Pentium M Processor 705	1.50GHz	600MHz	<b>1MB</b>	No	400MHz	130nm	July 2004
Intel Pentium M Processor 705a*	1.50GHz	600MHz	<b>1MB</b>	No	400MHz	130nm	November 2004
Intel Pentium M Processor 710	1.40GHz	600MHz	2MB	No	400MHz	90nm	October 2004
Intel Pentium M Processor 715	1.50GHz	600MHz	2MB	No	400MHz	90nm	June 2004
Intel Pentium M Processor 715a*	1.50GHz	600MHz	2MB	No	400MHz	90nm	January 2005
Intel Pentium M Processor 725	1.60GHz	600MHz	2MB	No	400MHz	90nm	June 2004
Intel Pentium M Processor 725a*	1.60GHz	600MHz	2MB	No	400MHz	90nm	June 2005
Intel Pentium M Processor 730	1.60GHz	<b>800MHz</b>	2MB	<b>Yes</b>	<b>533MHz</b>	90nm	January 2005
Intel Pentium M Processor 735	1.70GHz	600MHz	2MB	No	400MHz	90nm	May 2004
Intel Pentium M Processor 740	1.73GHz	<b>800MHz</b>	2MB	<b>Yes</b>	<b>533MHz</b>	90nm	January 2005
Intel Pentium M Processor 745	1.80GHz	600MHz	2MB	No	400MHz	90nm	May 2004
Intel Pentium M Processor 750	1.86GHz	<b>800MHz</b>	2MB	<b>Yes</b>	<b>533MHz</b>	90nm	January 2005
Intel Pentium M Processor 755	2.00GHz	600MHz	2MB	No	400MHz	90nm	May 2004
Intel Pentium M Processor 760	2.00GHz	<b>800MHz</b>	2MB	<b>Yes</b>	<b>533MHz</b>	90nm	January 2005
Intel Pentium M Processor 765	2.10GHz	600MHz	2MB	No	400MHz	90nm	October 2004
Intel Pentium M Processor 770	2.13GHz	<b>800MHz</b>	2MB	<b>Yes</b>	<b>533MHz</b>	90nm	January 2005
Intel Pentium M Processor 780	2.26GHz	<b>800MHz</b>	2MB	<b>Yes</b>	<b>533MHz</b>	90nm	July 2005

\*requires improved processor cooling because of higher Thermal Design Power

Code name	<b>Dothan</b> (705, 705a, 713, and 718 are Banias)
Branding	Part of the <b>Intel Centrino™ mobile technology</b> when included with an Intel 855 or 915 Express Chipset family and Intel PRO/Wireless Network Connection wireless chip
Micro-architecture	IA-32 / micro-op fusion, dedicated stack manager, advanced branch prediction, power-optimized processor system bus
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
Power mgmt technology	<b>Enhanced Intel SpeedStep™ technology</b> , Auto Halt, Stop Grant, Deep Sleep, Deeper Sleep
Hyper-Threading	No
Execute Disable Bit	<i>Some</i> : protects memory data areas from malicious software execution
EM64T	None
L1 cache - bus	256-bit data path / full speed
L1 data cache	32KB data cache / integrated
L1 instruction cache	32KB instruction cache / integrated
L2 cache - size	<b>1MB</b> or <b>2MB</b> / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (internal die; on die)
L3 cache	None
System bus	<b>400</b> or <b>533MHz</b> (transfers data 4 times per clock) / address bus transfers at 2 times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit
Out-of-order instructions	Yes (out-of-order instruction execution)
Branch prediction	Dynamic (based on history)
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Technology (micron)	0.09 micron or 90 nanometer ( <i>705, 705a, 713, and 718</i> : 0.13 micron or 130 nanometer)
Package and connector	<b>Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 478-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)</b>
Chipset support	<b>Intel 855, 910, and 915 Express Chipset family</b> <b>Other compatible chipsets</b>

**Intel® Celeron® D Processor for desktop systems**

	Clock speed	L2 cache	System bus	Execute Disable Bit	Hyper-Threading Technology	Enhanced Intel SpeedStep™ Technology	EM64T	Available date
Intel Celeron D Processor 320	2.40GHz	256KB	533MHz	No	No	No	No	June 2004
Intel Celeron D Processor 325	2.53GHz	256KB	533MHz	No	No	No	No	June 2004
Intel Celeron D Processor 325J	2.53GHz	256KB	533MHz	<b>Yes</b>	No	No	No	June 2004
Intel Celeron D Processor 326	2.53GHz	256KB	533MHz	<b>Yes</b>	No	No	<b>Yes</b>	May 2005
Intel Celeron D Processor 330	2.66GHz	256KB	533MHz	No	No	No	No	June 2004
Intel Celeron D Processor 330J	2.66GHz	256KB	533MHz	<b>Yes</b>	No	No	No	June 2004
Intel Celeron D Processor 331	2.66GHz	256KB	533MHz	<b>Yes</b>	No	No	<b>Yes</b>	May 2005
Intel Celeron D Processor 335	2.80GHz	256KB	533MHz	No	No	No	No	June 2004
Intel Celeron D Processor 335J	2.80GHz	256KB	533MHz	<b>Yes</b>	No	No	No	June 2004
Intel Celeron D Processor 336	2.80GHz	256KB	533MHz	<b>Yes</b>	No	No	<b>Yes</b>	May 2005
Intel Celeron D Processor 340	2.93GHz	256KB	533MHz	No	No	No	No	September 2004
Intel Celeron D Processor 340J	2.93GHz	256KB	533MHz	<b>Yes</b>	No	No	No	September 2004
Intel Celeron D Processor 341	2.93GHz	256KB	533MHz	<b>Yes</b>	No	No	<b>Yes</b>	May 2005
Intel Celeron D Processor 345	3.06GHz	256KB	533MHz	No	No	No	No	November 2004
Intel Celeron D Processor 345J	3.06GHz	256KB	533MHz	<b>Yes</b>	No	No	No	November 2004
Intel Celeron D Processor 346	3.06GHz	256KB	533MHz	<b>Yes</b>	No	No	<b>Yes</b>	May 2005
Intel Celeron D Processor 350	3.20GHz	256KB	533MHz	<b>Yes</b>	No	No	No	June 2005
Intel Celeron D Processor 351	3.20GHz	256KB	533MHz	<b>Yes</b>	No	No	<b>Yes</b>	June 2005

Processor generation	Prescott
Core	Based on Prescott (Pentium 4) core
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Hyper-Threading	No
Execute Disable Bit	<i>Some:</i> protects memory data areas from malicious software execution
EM64T	<i>Some:</i> Extended Memory 64 Technology

L1 cache - bus	256-bit data path / full speed
L1 data cache	16KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)

L2 cache - size	<b>256KB</b> / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None

System bus	<b>533MHz</b> (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
System bus - width	64-bit data path

Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit
Out-of-order instructions	Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers

Compatibility	Compatible with IA-32 software (some compatible with EM64T software)
Other features	Thermal monitoring, built-in self test, IEEE 1149.1 standard test access port and boundary scan

Technology	90nm (nanometer) or 0.09u (micron)
Package and socket	<b>All: Flip-Chip Pin Grid Array (FC-mPGA4) package requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket</b> <b>All except 320 and 350: 775-land Flip-Chip Land Grid Array (FC-LGA4) package requires LGA775 socket (socket also called Socket T)</b>
Chipset support	<i>FC-mPGA4 package:</i> Intel 845 family, 848P, 865 family, 910, or other compatible chipsets <i>FC-LGA4 package:</i> Intel 910 and 915 Express Chipset family

# [Desktop] Intel Pentium 4 Processor (Northwood)

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## Intel® Pentium® 4 for high performance desktop systems

Code name	<b>Northwood</b>
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
Hyper-Threading	3.06GHz with 533MHz and all 800MHz system bus processors: Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	<b>512KB</b> / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None
System bus	<b>400 or 533 or 800MHz</b> (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
Frontside bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Multiple processors	No SMP support
Technology (micron)	0.13u
Transistors	~55 million
Package and connector	<b>Flip-Chip Pin Grid Array-2 (FC-PGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket</b>
Frequency and available date	1.6GHz sub-45W TDP (limited to under 45 watts thermal design point; for small form factor desktops); avail Jan 2002 1.8GHz sub-45W TDP (limited to under 45 watts thermal design point; for small form factor desktops); avail Jan 2002 2.0GHz sub-45W TDP (limited to under 45 watts thermal design point; for small form factor desktops); avail Jan 2002 1.8A GHz with 400MHz system bus: available July 2002 2.0A GHz with 400MHz system bus: available January 2002 ("A" signifies the 0.13 micron version, not 0.18 micron) 2.2GHz with 400MHz system bus: available January 2002 2.26GHz with 533MHz system bus: available May 2002 2.4GHz with 400MHz system bus: available April 2002 2.4B GHz with 533MHz system bus: available May 2002 2.4C GHz with 800MHz system bus: available May 2003 with Hyper-Threading Technology 2.5GHz with 400MHz system bus: available August 2002 2.53GHz with 533MHz system bus: available May 2002 2.6GHz with 400MHz system bus: available August 2002 2.6C GHz with 800MHz system bus: available May 2003 with Hyper-Threading Technology 2.66GHz with 533MHz system bus: available August 2002 2.8GHz with 400MHz system bus: available April 2003 (used in ThinkPad G40) 2.8GHz with 533MHz system bus: available August 2002 2.8C GHz with 800MHz system bus: available May 2003 with Hyper-Threading Technology 3.0GHz with 800MHz system bus: available April 2003 with Hyper-Threading Technology 3.0GHz with 400MHz system bus: available April 2003 (used in ThinkPad G40) 3.06GHz with 533MHz system bus: available November 2002 with Hyper-Threading Technology 3.2GHz with 800MHz system bus: available June 2003 with Hyper-Threading Technology 3.4GHz with 800MHz system bus: available February 2004 with Hyper-Threading Technology
Chipset support	Intel 850 or 850E with dual channel RDRAM memory Intel 845 with SDRAM or DDR-SDRAM memory Intel 865 family with single or dual channel DDR-SDRAM memory (400, 533, or 800 MHz system bus) Intel 875P with single or dual channel DDR-SDRAM memory (800 MHz system bus)

# [Desktop] Intel Pentium 4 Processor (Prescott)

Created by PC Institute  
Personal Systems Reference (PSREF)

## Intel® Pentium® 4 for desktop systems

Code name	<b>Prescott</b>	
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)	
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)	
SSE2	Streaming SIMD Extensions 2 (144 new instructions)	
SSE3	Streaming SIMD Extensions 3 (13 new instructions)	
Hyper-Threading	800MHz system bus processors: Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)	
L1 cache - bus	256-bit data path / full speed	
L1 data cache	16KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated	
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)	
L2 cache - size	<b>1MB</b> / full speed (Advanced Transfer Cache)	
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC	
L3 cache	None	
System bus	<b>533</b> or <b>800MHz</b> (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size	
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz	
System bus - width	64-bit data path	
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)	
Out-of-order instructions	Yes	
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer	
Speculative execution	Yes (Advanced Dynamic Execution)	
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers	
Compatibility	Compatible with IA-32 software	
Multiple processors	No SMP support	
Other features	Thermal monitoring, built-in self test, IEEE 1149.1 standard test access port and boundary scan	
Technology	90nm (nanometer) or 0.09u (micron)	
Package and connector	<b>Flip-Chip Pin Grid Array (FC-mPGA4) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket</b>	
Frequency and available date	<b>2.80A</b> GHz with 533MHz system bus <b>2.80E</b> GHz with 800MHz system bus with Hyper-Threading Technology <b>3.00E</b> GHz with 800MHz system bus with Hyper-Threading Technology <b>3.20E</b> GHz with 800MHz system bus with Hyper-Threading Technology <b>3.40E</b> GHz with 800MHz system bus with Hyper-Threading Technology	available February 2004 available February 2004 available February 2004 available February 2004 available February 2004
Chipset support	Intel 865 family with single or dual channel DDR-SDRAM memory Intel 875P with single or dual channel DDR-SDRAM memory	

# [Desktop] Intel Pentium 4 Processor 5xx

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<i>Intel® Pentium® 4 for desktop systems</i>		Clock speed	L2 cache	Execute Disable Bit	System bus	Hyper-Threading Technology	Enhanced Intel SpeedStep™	EM64T	Available date
Intel Pentium 4 Processor 506		2.66GHz	1MB	Yes	533MHz	No	No	Yes	Jul 05
Intel Pentium 4 Processor 515		2.93GHz	1MB	No	533MHz	No	No	No	Nov 04
Intel Pentium 4 Processor 516		2.93GHz	1MB	No	533MHz	No	No	Yes	Jun 05
Intel Pentium 4 Processor 519		3.06GHz	1MB	Yes	533MHz	No	No	Yes	Jul 05
Intel Pentium 4 Processor supporting Hyper-Threading Technology 520		2.8GHz	1MB	No	800MHz	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 520J		2.8GHz	1MB	Yes	800MHz	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 521		2.8GHz	1MB	Yes	800MHz	HT	No	Yes	May 05
Intel Pentium 4 Processor supporting Hyper-Threading Technology 530		3.0GHz	1MB	No	800MHz	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 530J		3.0GHz	1MB	Yes	800MHz	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 531		3.0GHz	1MB	Yes	800MHz	HT	No	Yes	May 05
Intel Pentium 4 Processor supporting Hyper-Threading Technology 540		3.2GHz	1MB	No	800MHz	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 540J		3.2GHz	1MB	Yes	800MHz	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 541		3.2GHz	1MB	Yes	800MHz	HT	No	Yes	May 05
Intel Pentium 4 Processor supporting Hyper-Threading Technology 550		3.4GHz	1MB	No	800MHz	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 550J		3.4GHz	1MB	Yes	800MHz	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 551		3.4GHz	1MB	Yes	800MHz	HT	No	Yes	May 05
Intel Pentium 4 Processor supporting Hyper-Threading Technology 560		3.6GHz	1MB	No	800MHz	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 560J		3.6GHz	1MB	Yes	800MHz	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 561		3.6GHz	1MB	Yes	800MHz	HT	No	Yes	May 05
Intel Pentium 4 Processor supporting Hyper-Threading Technology 570J		3.8GHz	1MB	Yes	800MHz	HT	No	No	Nov 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 571		3.8GHz	1MB	Yes	800MHz	HT	No	Yes	May 05

Code name	<b>Prescott</b>
Core	Single-core
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Hyper-Threading	<i>Some:</i> Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
Execute Disable Bit	<i>Some:</i> protects memory data areas from malicious software execution
EM64T	<i>Some:</i> Extended Memory 64 Technology
L1 cache - bus	256-bit data path / full speed
L1 data cache	16KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	<b>1MB</b> / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None
System bus	<b>533 or 800MHz</b> (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software (some compatible with EM64T software)
Other features	Thermal monitoring, built-in self test, IEEE 1149.1 standard test access port and boundary scan
Technology	90nm (nanometer) or 0.09u (micron)
Package and socket	<b>775-land Flip-Chip Land Grid Array (FC-LGA4) package requires LGA775 socket</b> (socket also called Socket T)
Chipset support	Intel 915G, 915GV, 915P, 925X, and 925XE Express chipset or other compatible chipsets

# [Desktop] Intel Pentium 4 Processor 6xx

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## Intel® Pentium® 4 supporting Hyper-Threading Technology for desktop systems

	Clock speed	L2 cache	Core	System bus	Execute Disable Bit	Hyper-Threading Technology	Enhanced Intel SpeedStep™ Technology	EM64T¹	Available date
Intel Pentium 4 Processor 630	3.00GHz	2MB	Single	800MHz	XD	HT	EIST	EM64T	Feb 2005
Intel Pentium 4 Processor 640	3.20GHz	2MB	Single	800MHz	XD	HT	EIST	EM64T	Feb 2005
Intel Pentium 4 Processor 650	3.40GHz	2MB	Single	800MHz	XD	HT	EIST	EM64T	Feb 2005
Intel Pentium 4 Processor 660	3.60GHz	2MB	Single	800MHz	XD	HT	EIST	EM64T	Feb 2005
Intel Pentium 4 Processor 670	3.80GHz	2MB	Single	800MHz	XD	HT	EIST	EM64T	May 2005

Code name	<b>Prescott</b>
Core	Single core
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Power mgmt technology	Enhanced Intel SpeedStep™ Technology
Hyper-Threading	Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
EM64T	Extended Memory 64 Technology
L1 cache - bus	256-bit data path / full speed
L1 data cache	16KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	<b>2MB</b> / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None
System bus	<b>800MHz</b> (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 and EM64T software
Other features	Thermal monitoring, built-in self test, IEEE 1149.1 standard test access port and boundary scan
Technology	90nm (nanometer) or 0.09u (micron)
Package and socket	<b>775-land Flip-Chip Land Grid Array (FC-LGA4) package requires LGA775 socket</b> (socket also called Socket T)
Chipset support	Intel 915 chipset family, 925X, 925XE, 945 chipset family, 955X, or other compatible chipsets

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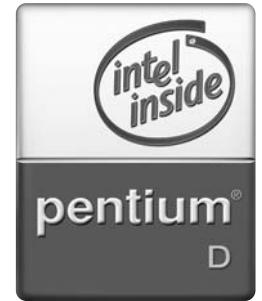
# [Desktop] Intel Pentium D Processor 8xx

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## Intel® Pentium® Processor D Processor for desktop systems

	Clock speed	L2 cache	System bus	Package	Core	Hyper-Threading Technology	Total threads (logical)	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	EM64T	Available date
Pentium D Processor 820	2.80GHz	2x1MB	800MHz	FC-LGA4	Dual	No	2	Yes	No	EM64T	Jun 05
Pentium D Processor 830	3.00GHz	2x1MB	800MHz	FC-LGA4	Dual	No	2	Yes	Yes	EM64T	Jun 05
Pentium D Processor 840	3.20GHz	2x1MB	800MHz	FC-LGA4	Dual	No	2	Yes	Yes	EM64T	Jun 05

Processor generation	Smithfield
Core	Dual-core
Formal name	<b>Intel Pentium D Processor</b>
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Power mgmt technology	<i>Some:</i> Enhanced Intel SpeedStep™ Technology
Hyper-Threading	No
Total threads	Two threads (two cores with no Hyper-Threading support provide two logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
EM64T	Extended Memory 64 Technology (an extension to the IA-32 instruction set which adds 64 bit extensions to the x86 architecture)



L1 cache - bus	256-bit data path / full speed
L1 data cache	Two 16KB data caches / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / two instruction caches (each hold 12,000 micro-ops) / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	<b>Two 1MB</b> (one for each core) / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None
System bus	<b>800MHz</b> (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
Frontside bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 and EM64T software
Technology (micron)	90nm or 0.09u
Package and connector	<b>775-land Flip-Chip Land Grid Array (FC-LGA4) package requires LGA775 socket</b> (socket also called Socket T)
Chipset support	Intel 945 Express chipset family, 955X Express chipset

# [Desktop] Intel Pentium 4 Processor Extreme Edition

Created by PC Institute  
Personal Systems Reference (PSREF)

## Intel® Pentium® 4 Processor Extreme Edition for high-end gamers and power users

	Clock speed	L2 cache	L3 cache	System bus	Core	Package	Execute Disable Bit	Hyper-Threading Technology	Enhanced Intel SpeedStep™ Technology	EM64T	Available date
Intel Pentium 4 Processor Extreme Edition	3.2GHz	512KB	2MB	800MHz	Single	FC-PGA2	No	HT	No	No	Nov 03
Intel Pentium 4 Processor Extreme Edition	3.4GHz	512KB	2MB	800MHz	Single	FC-PGA2	No	HT	No	No	Feb 04
Intel Pentium 4 Processor Extreme Edition	3.4GHz	512KB	2MB	800MHz	Single	FC-LGA4	No	HT	No	No	Jun 04
Intel Pentium 4 Processor Extreme Edition	3.46GHz	512KB	2MB	1066MHz	Single	FC-LGA4	No	HT	No	No	Nov 04
Intel Pentium 4 Processor Extreme Edition	3.73GHz	2MB	None	1066MHz	Single	FC-LGA4	Yes	HT	No	Yes	Feb 05

Code name	None (3.73GHz is Prescott)
Core	Single core
Formal name	<b>Intel Pentium 4 Processor with HT Technology Extreme Edition</b>
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	<i>3.73GHz only:</i> Streaming SIMD Extensions 3 (13 new instructions)
Power mgmt technology	None
Hyper-Threading	Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
Execute Disable (XD) Bit	<i>3.73GHz only:</i> protects memory data areas from malicious software execution
EM64T	<i>3.73GHz only:</i> Extended Memory 64 Technology



L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	<b>512KB or 2MB</b> / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	<i>Some:</i> None <i>Some:</i> <b>2MB</b> / full speed / 256-bit data path (32 bytes) / transfers on each bus clock / 64 byte cache line size / 8-way set associative / write-back / parity / integrated / unified (internal die; on die)
System bus	<b>800MHz or 1066MHz</b> (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
Frontside bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software (some compatible with EM64T software)
Multiple processors	No SMP support
Technology (micron)	0.13u (3.73GHz is 90nm or 0.09u)
Package and connector	<b>Flip-Chip Pin Grid Array-2 (FC-PGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket or 775-land Flip-Chip Land Grid Array (FC-LGA4) package requires LGA775 socket</b> (socket also called Socket T)
Chipset support	Intel 848P, 865 family, and 875P for FC-PGA2 package Intel 915G, 915P, 925X, and 925XE Express chipset for FC-LGA4 package Intel 925XE Express supports 1066MHz system bus

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- <sup>1</sup> **EM64T:** Intel Extended Memory 64 Technology (Intel EM64T) requires a computer system with a processor, chipset, BIOS, operating system, device drivers, and applications enabled for Intel EM64T. Processor will not operate (including 32-bit operation) without an Intel EM64T-enabled BIOS. Performance will vary depending on your hardware and software configurations.

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August 2005  
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